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Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1. – 18. (cancelled)

19. (previously presented) An integrated circuit device comprising:
a first clock data recovery (CDR) circuit to recover clock and data signals from a first signal line, the first CDR circuit including:
a first phase control circuit to generate a first control signal, and
a first phase adjust circuit to adjust the phase of a first recovered clock signal in response to the first control signal; and
a second CDR circuit to recover clock and data signals from a second signal line, the second CDR circuit including:
a second phase control circuit to generate a second control signal,
a select circuit coupled to receive the first and second control signals and being responsive to a select signal to select from one of the first control signal and the second control signal to be output as a selected control signal, and
a second phase adjust circuit to adjust the phase of a second recovered clock signal in response to the selected control signal.

20. (previously presented) The integrated circuit device of claim 19 wherein the select circuit comprises a multiplexer circuit having a control input coupled to receive the select signal and having respective input ports coupled to receive the first and second control signals from the first and second phase control circuits.

21. (previously presented) The integrated circuit device of claim 19 further comprising additional CDR circuits each having a respective phase control circuit, select circuit and phase adjust circuit, the select circuit of each of the additional CDR circuits being responsive to a control input to output, as a selected control signal, from one of the first control signal and a phase control signal output by the phase control circuit of the additional CDR circuit, the phase adjust circuit of each of the additional CDR circuits

being responsive to the selected control signal output by the select circuit for the additional CDR circuit to adjust the phase of a respective recovered clock signal.

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22. (previously presented) The integrated circuit device of claim ~~19~~ wherein the first CDR circuit further includes a first receive circuit to sample an input signal on the first signal line in response to the first recovered clock signal, and the second CDR circuit further includes a second receive circuit to sample an input signal on the second signal line in response to the second recovered clock signal.

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23. (previously presented) The integrated circuit device of claim ~~19~~ further comprising an input to receive the select signal from an external device.

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24. (previously presented) The integrated circuit device of claim ~~19~~ further comprising a programmable register to store a mode value, the select signal having from one of a first state and a second state according to the mode value, and the select circuit including a circuitry to select the first control signal when the select signal is in the first state and to select the second control signal when the select signal is in the second state.

7 1
25. (previously presented) The integrated circuit device of claim ~~19~~ wherein the select circuit is responsive to the select signal to disable generation of the first control signal when the select signal indicates that the select circuit is to select the second control signal to be output as the selected control signal.

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26. (previously presented) A method of controlling an integrated circuit, the method comprising:

outputting a first command to the integrated circuit to set a first clock data recovery (CDR) circuit within the integrated circuit to a first mode, the first CDR circuit including a select circuit to select a first control signal to adjust the phase of a first clock signal when the first CDR circuit is in the first mode;

delaying for a first time interval; and

outputting, after the first time interval, a second command to the integrated circuit to set the first CDR circuit to a second mode, the select circuit of the first CDR circuit to select

a second control signal when the first CDR circuit is in the second mode, the second control signal being generated by a second CDR circuit.

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27. (previously presented) The method of claim ~~26~~ wherein delaying for the first time interval comprises delaying until a predetermined number of cycles of a clock signal have transpired.

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28. (previously presented) The method of claim ~~26~~ wherein outputting the first command to the integrated circuit to set the first CDR circuit to the first mode comprises outputting a command to the integrated circuit to store a mode value in a programmable register within the integrated circuit, the mode value indicating the first mode.

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29. (previously presented) The method of claim ~~26~~ wherein outputting the first command to the integrated circuit to set the first CDR circuit to the first mode comprises outputting a mode signal to the integrated circuit, the mode signal being input to a select input of the select circuit to select the first control signal.

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30. (previously presented) The method of claim ~~26~~ further comprising periodically repeating the outputting the first command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

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31. (previously presented) The method of claim ~~26~~ further comprising:
detecting a predetermined condition; and
in response to the detecting the predetermined condition, repeating the outputting the first command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

14 13
32. (previously presented) The method of claim ~~31~~ wherein the detecting the predetermined condition comprises detecting a change in temperature.

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33. (previously presented) The method of claim ~~31~~ wherein the detecting the predetermined condition comprises detecting a change in voltage.

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34. (previously presented) The method of claim 31 wherein the detecting the predetermined condition comprises detecting a loss of synchronization between the first clock signal and a data signal received in the first CDR circuit.

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35. (currently amended) A system comprising:

a first signal line;

a receive device coupled to the first signal line, the receive device having a first clock data recovery (CDR) circuit to recover clock and data signals from the first signal line, the first CDR circuit including a control circuit, a select circuit and a phase adjust circuit, the control circuit to generate a first control signal according to a phase relationship between an input signal on the first signal line and a first clock signal, the select circuit being responsive to a first mode value to select from one of the first control signal and a second control signal to be output as a selected control signal, the phase adjust circuit to adjust the phase of the first clock signal according to the selected control signal; ~~and~~

a control device coupled to the receive device to provide the first mode value; and

at least one additional signal line, the at least one additional signal line coupled to the receive device and to the control device, the control device provides the first mode value to the receive device via the at least one additional signal line.

18 17
36. (previously presented) The system of claim 35 wherein the control device is coupled to provide the first mode value to the receive device via the first signal line.

37. (cancelled)

19 17
38. (currently amended) The system of claim 35 wherein the control device ~~to output~~ outputs the first mode value to the receive device and then, after a first time interval, ~~to output~~ outputs a second mode value to the receive device, the select circuit being responsive to the first mode value to select the first control signal to be output as the selected control signal, the select circuit being responsive to the second mode value to select the second control signal to be output as the selected control signal.

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39. (currently amended) ~~The system of claim 38~~ A system comprising:

a first signal line;

a receive device coupled to the first signal line, the receive device having a first clock data recovery (CDR) circuit to recover clock and data signals from the first signal line, the first CDR circuit including a control circuit, a select circuit and a phase adjust circuit, the control circuit to generate a first control signal according to a phase relationship between an input signal on the first signal line and a first clock signal, the select circuit being responsive to a first mode value to select from one of the first control signal and a second control signal to be output as a selected control signal, the phase adjust circuit to adjust the phase of the first clock signal according to the selected control signal;

a control device coupled to the receive device to provide the first mode value;

wherein the control device outputs the first mode value to the receive device and then, after a first time interval, outputs a second mode value to the receive device, the select circuit being responsive to the first mode value to select the first control signal to be output as the selected control signal, the select circuit being responsive to the second mode value to select the second control signal to be output as the selected control signal; and

~~further comprising~~ a second signal line coupled to the receive device, and wherein the receive device includes a second CDR circuit to recover clock and data signals from the second signal line, the second CDR circuit including a control circuit to generate the second control signal according to a phase relationship between an input signal on the second signal line and a second clock signal.

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40. (previously presented) The system of claim ~~35~~ wherein the receive device is implemented in a first integrated circuit and the control device is implemented in a second integrated circuit.

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41. (previously presented) The system of claim ~~40~~ wherein the first and second integrated circuits are packaged in separate integrated circuit packages.

22 20
42. (previously presented) The system of claim ~~40~~ wherein the first and second integrated circuits are packaged in the same integrated circuit package.

23 17
43. (previously presented) The system of claim ~~35~~ wherein the receive device and the control device are implemented within a single integrated circuit.

44. (cancelled)

25
45. (previously presented) A method of testing an integrated circuit (IC) that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:
outputting a command to the IC to set the CDR circuit to a mode of operation, the CDR circuit having a select circuit that responds to the mode of operation by selecting the phase control port to source a control signal instead of a phase control circuit within the CDR circuit, the control signal used by a phase adjust circuit within the CDR circuit to adjust the phase of a clock signal;
outputting a phase control signal to the phase control port of the integrated circuit device to adjust the phase of the clock signal; and
wherein outputting the first command to the integrated circuit to set the CDR circuit to the mode of operation comprises outputting a command to the integrated circuit to store a mode value in a programmable register within the integrated circuit, the mode value indicating the mode of operation.

46. (cancelled)

26
47. (previously presented) A method of testing an integrated circuit (IC) that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:
outputting a command to the IC to set the CDR circuit to a mode of operation, the CDR circuit having a select circuit that responds to the mode of operation by selecting the phase control port to source a control signal instead of a phase control circuit within the CDR circuit, the control signal used by a phase adjust circuit within the CDR circuit to adjust the phase of a clock signal;

asserting a phase control signal at the phase control port of the integrated circuit for a first predetermined time interval, the phase adjust circuit within the CDR circuit responsive to the phase control signal to adjust the phase of the clock signal;

deasserting the phase control signal for a second predetermined time interval; and

measuring the clock signal with a signal measuring device while repeating asserting a phase control signal and deasserting the phase control signal at least until the phase of the clock signal has progressed through a predetermined portion of a cycle of the clock signal.

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48. (previously presented) The method of claim ~~47~~ 26 wherein the predetermined portion of a cycle of the clock signal is an entire cycle of the clock signal.

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49. (previously presented) The method of claim ~~47~~ 26 wherein the phase adjust circuit responds to assertion of the control signal by advancing the phase of the clock signal.

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50. (previously presented) The method of claim ~~47~~ 26 wherein the first predetermined time interval is selected to allow the phase adjust circuit to advance the phase of the clock signal by a predetermined phase angle.

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51. (previously presented) The method of claim 47 26 wherein measuring the clock signal with a signal measuring device comprises measuring the clock signal with an oscilloscope.

52. – 58. (cancelled)

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59. (previously presented) A method of testing an integrated circuit that includes a clock data recovery (CDR) circuit and a phase control port, the method comprising:

setting the CDR circuit to a test mode in which a select circuit within the CDR circuit selects the phase control port to source a control signal instead of a phase control circuit within the CDR circuit, the control signal used by a phase adjust circuit within the CDR circuit to adjust the phase of a first clock signal;

inputting a test signal to a receiver of the CDR circuit;

comparing the test signal against samples of the test signal generated by the CDR circuit;

asserting an error signal when the test signal does not match the samples;

asserting a phase control signal at the phase control port to adjust the phase of the first clock signal; and

repeating comparing the test signal, asserting an error signal and asserting a phase control signal to determine a maximum phase and a minimum phase of the first clock signal for which the error signal is not asserted.